CLAIM

What is claimed is:

1. A mixed Q-nary and carry line digital engineering method, comprising the following steps:

The first step, add a numeral sign to each bit of numeral of the common Q-nary numerals that participate in the operation, i.e., indicating if said bit of numeral is positive or negative, so as to make it become a mixed Q-nary numeral, suppose that the numerals that participate in the operation are k mixed Q-nary numerals:

The second step, perform a sum operation for k numerals at the same time, the operation starts from the lowest bit, and the numerals are added by bit, that is, at a certain bit, two numerals in said k numerals are taken to be added by bit, and a "sum by bit" is obtained, which is the sum of operation layer as the "partial sum" numeral, meanwhile, the obtained "mixed numeral scale" is stored at the higher bit adjacent to said bit in any carry line in the next operation layer;

The third step, chose other two numerals among the k numerals at said bit to perform the second step of operation, and repeat these steps until the k numerals are all taken; when there is only one numeral of the k numerals left, it is directly moved to the same bit at the next operation layer as the "partial sum" numeral;

The fourth step, at a higher bit adjacent to the above-mentioned certain bit, the operations of the second and third steps are repeated until all the operations of each bit of the k operational numerals are finished;

The fifth step, in the next operation layer, an operation for the sum as described in the previous second, third and fourth steps is performed for said "sum by bit" numeral and the "carry numeral" in the carry line;

The operations of the second to the fifth steps are repeated until no "mixed Q-nary" is produced, then the sum obtained in the last "adding by bit" is the result of the addition.

2. The mixed Q-nary and carry line digital engineering method according to claim 1, characterized by that at a certain bit, when performing sum operation for two numerals of the k numerals, if two numerals of said bit are opposite numerals, then the sum of said bit is zero, then a certain bit of said two operational numerals are set to be "0" in a logic manner and they will not participate in future operations; when performing sum operation for two numerals of the k numerals at a certain bit, if the sum of adding by bit of two numerals is zero, but the carry is produced, then the carry is put to the adjacent higher bit in any carry line, and a certain bit of said two operational numerals are set to be "0" in a logic manner and they will not participate in future operations.

3. The mixed Q-nary and carry line digital engineering method according to claim 1 or 2, characterized by that the mixed Q-nary numeral is encoded by all one code, that is, each bit of numeral S of the mixed Q-nary numerals is represented by 1 with the number of S arranged from the lowest bit to the higher bit, and the rest of the higher bits are all 0, and the total number of bits are (Q-1); meanwhile, the numeral sign of said bit, i.e., the sign indicating if the numeral of said bit is positive or negative, is used as the numeral sign of each bit in the corresponding all one code.

4. The mixed Q-nary and carry line digital engineering method according to any one of claims 1 to 3, characterized by that addition of two numerals is only the non-repeated arrangement of 1 of the two numerals.

5. The mixed Q-nary and carry line digital engineering method according to claim 1 or 2, wherein said operational numeral is mixed Q-nary numeral, Q is natural number.

6. The mixed Q-nary and carry line digital engineering method according to claim 1 or 2, wherein said operational numeral is common mixed Q-nary numeral, in particular common mixed ternary numeral.

7. The mixed Q-nary and carry line digital engineering method according to claim 1 or 2, wherein said operational numeral is numeral of the mixed numeral numerical system.

8. A mixed Q-nary and carry line processor, comprising input logic (101), K-layer arithmetic unit (202), output transformation logic (108) and controller (201); the mixed Q-nary numeral shift register inputs logic (101) to the K-layer arithmetic unit (202); in the K-layer arithmetic unit (202), a mixed Q-nary numeral result is obtained for the mixed Q-nary numeral after the K-layer operations, which is output by the output logic (104) through the decoder output transformation logic (108) in the form of Q-nary numeral or mixed Q-nary numeral, or common decimal numeral, the controller (201) coordinates and controls the logic of the entire operation controller; wherein,

each register of the 2K registers and each bit of the accumulator are assigned with a sign bit, said sign bit is a common two-state trigger; the former K registers store the inputted K mixed-Q numerals, while the latter K registers form the K carry lines;

During operation, a certain bit of two registers obtains the sum thereof and the carry for the higher bit after the accumulator accumulates them, and the carry is sent to the adjacent higher bit of any carry line register; when the next operation command arrives, the carry line and the originally stored numeral are sent to the accumulator to added;

such processes are repeated and finally the sum is obtained by the accumulator.

9. The mixed Q-nary and carry line processor according to claim 8, further comprising:

counterpart scratching network (312) and scratching Q network (313) connect to the register in the register network (311) two by two;

instructions sent by the controller or program first perform "counterpart scratching" and "scratching Q" operations on each numeral of the operational numerals at a certain bit, then perform accumulation operation; wherein the accumulator (304) is a common accumulator

with each bit thereof having a positive or negative sign bit;

the "carry" produced by scratching Q at a certain bit is sent to the "1" end of the adjacent higher bit of the register of any carry line in the K-layer arithmetic unit.

10. The mixed Q-nary and carry line processor according to claim 9, wherein the counterpart scratching network (312) is inspected by the counterpart scratching logic (305), or it is formed by connecting the K (2K-1) counterpart scratching logic (305, 306...307) to the registers in the register network (311) two by two; or it is formed by grouped or graded counterpart scratching logic;

wherein the scratching Q network (313) is inspected by a scratching Q logic (310), or is formed by connecting the K (2K-1) scratching Q logic (308, 309...310) to the registers in the register network (311) two by two; or it is formed by grouped or graded scratching Q logic;

in said "K-layer arithmetic unit", if the value of K is large, a graded amplification could be performed thereon.

11. The mixed Q-nary and carry line processor according to claim 10, wherein the counterpart scratching logic is composed of the ith bit (401) of register A, the ith bit (402) of register B, equivalent logic (403), non-equivalent logic (404) and AND gate (405), wherein a sign bit is attached before the ith bit (401) of register A, which is a common two-state trigger, wherein the "1" end of Ai is connected to the input of the equivalent logic (403), and the "1" end of the Ai sign is connected to the input of the non-equivalent logic (404); a sign bit is attached before the ith bit (402) of the register B, which is a common two-state trigger, wherein the "1" end of Bi is connected to the input of the equivalent logic (403), and the "1" end of the Bi sign is connected to the input of the non-equivalent logic (404). The output of the equivalent logic (403) is connected to the input of the AND gate (405); the output of the non-equivalent logic (404) is connected to the input of the AND gate (405); and the output of the AND gate (405) is connected to the setting "0" end of the ith bit (401) of register A and the setting "0" end of the ith bit (402) of register B.

wherein the scratching Q logic is composed of ith bit (501) of register A, the ith bit (502) of register B, Q value determination logic (503), equivalent logic (504) and AND gate (505),

wherein a sign bit is attached before the ith bit (501) of register A, which is a common two-state trigger; the "1" end of Ai is connected to the input of the Q value determination logic (503), and the "1" end of the Ai sign is connected to the input of the equivalent logic (504); a sign bit is attached before the ith bit (502) of register B, which is a common two-state trigger; the "1" end of Bi is connected to the input of the Q value decision logic (503); the "1" end of the Bi sign is connected to the input of the equivalent logic (504); the output of the Q value decision logic (503) is connected to the input of the AND gate (505); the output of the equivalent logic (504) is connected to the input of the AND gate (505); the output of the AND gate (505) is connected to the setting "0" end of the ith bit (501) of register A and the setting "0" end of the ith bit (502) of register B.

12. The mixed Q-nary and carry line processor according to claim 8, wherein said operational numeral is represented by all one code.

13. The mixed Q-nary and carry line processor according to claim 8, wherein said operational numeral is mixed Q-nary numeral, and Q is natural number.

14. The mixed Q-nary and carry line processor according to claim 8, wherein said operational numeral is common Q-nary numeral.

15. The mixed Q-nary and carry line processor according to claim 8, wherein said operational numeral is numeral of the mixed numeral numerical system.